WHAT IS CLAIMED IS:

1. A circuit comprising:

a plurality of memory modules;

a memory controller coupled to the plurality of memory modules;

a plurality of bus splitters coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller; and

a plurality of terminators to reduce signal reflections corresponding to the split signals.

2. The circuit of claim 1 wherein the plurality of terminators are embedded in each of the plurality of memory modules.

3. The circuit of claim 1 wherein the plurality of terminators are embedded in the memory controller.

4. The circuit of claim 1 wherein the memory modules are dual in-line memory modules (DIMMs).

5. The circuit of claim 1 further including a reference voltage generator to generate a reference voltage corresponding to a memory chip voltage.

6. The circuit of claim 5 wherein the reference voltage is provided to the plurality of memory modules and the memory controller.

7. The circuit of claim 1 wherein the plurality of bus splitters are one or more items selected from a group comprising miniature resistive splitters on a PCB and miniature integrated resistor packs.

8. The circuit of claim 1 further including a plurality of memory expander chips (MXCs) coupled between the memory controller and the plurality of memory modules.

9. The circuit of claim 8 wherein the plurality of MXCs enable access to relative larger memory arrays.

10. The circuit of claim 8 wherein each of the plurality of MXCs include one or more items selected from a list comprising a micro-controller to perform tasks locally and a built in bi-directional cache to decrease latency and increase throughput efficiency.

11. The circuit of claim 8 wherein a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs.

12. The circuit of claim 8 wherein each of the plurality of MXCs include functionality selected from a group comprising local refresh generation, dynamic address space re-mapping, access re-ordering, access coalescing, memory power-on self-test (POST), and local management of open pages.

13. The circuit of claim 8 wherein a portion of the plurality of MXCs are coupled to each other in series.

14. A method comprising:

providing a plurality of memory modules;

coupling a memory controller to the plurality of memory modules;

coupling a plurality of bus splitters between the plurality of memory modules and the memory controller to split signals communicated between the

plurality of memory modules and the memory controller; and

providing a plurality of terminators to reduce signal reflections corresponding to the split signals.

15. The method of claim 14 wherein the plurality of terminators are embedded in each of the plurality of memory modules.

16. The method of claim 14 wherein the plurality of terminators are embedded in the memory controller.

17. The method of claim 14 wherein the memory modules are dual in-line memory modules (DIMMs).

18. The method of claim 14 further including generating a reference voltage corresponding to a memory chip voltage.

19. The method of claim 18 wherein the reference voltage is provided to the plurality of memory modules and the memory controller.

20. The method of claim 14 wherein the plurality of bus splitters are one or more items selected from a group comprising miniature resistive splitters on a PCB and miniature integrated resistor packs.

21. The method of claim 14 further including coupling a plurality of memory expander chips (MXCs) between the memory controller and the plurality of memory modules.

22. The method of claim 21 wherein the plurality of MXCs enable access to relatively larger memory arrays.

23. The method of claim 21 wherein each of the plurality of MXCs include one or more items selected from a list comprising a micro-controller to perform tasks locally and a built in bi-directional cache to decrease latency and increase throughput efficiency.

24. The method of claim 21 wherein a data rate between the memory controller and the plurality of MXCs runs at a relatively higher bandwidth than that of directly supported DIMMs.

25. The method of claim 21 wherein each of the plurality of MXCs include functionality selected from a group comprising local refresh generation, dynamic address space re-mapping, access re-ordering, access coalescing, memory power-on self-test (POST), and local management of open pages.

26. The method of claim 21 wherein a portion of the plurality of MXCs are coupled to each other in series.

27. A computer system comprising:

a central processing unit (CPU);

a display device coupled to the CPU to display an image;

a plurality of memory modules;

a memory controller coupled to the plurality of memory modules and the CPU;

a plurality of bus splitters coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller; and

a plurality of terminators to reduce signal reflections corresponding to the split signals.

28. The computer system of claim 27 further including a main memory coupled to the CPU.

29. The computer system of claim 27 further including a memory coupled to the display device to store the image.

30. The computer system of claim 27 wherein the memory controller is coupled to the CPU through a memory control hub.